CLAIMS

1. An active matrix display device comprising an array of pixels (P) a set of row conductors (14) through which rows of pixels are selected, a set of column conductors (5) through which data signals are supplied to selected pixels, each pixel (P) comprising a plurality of sub pixels (P1 – P4), which sub pixels are each associated with a respective switching transistor (T1 – T4) for controlling the supply of a data signal to the sub pixel,

wherein the plurality of sub pixels of a pixel are coupled to a column conductor (15) associated with the pixel via a common switching transistor (T1) through which data signals are supplied to the sub pixels, and wherein the device is operable in a first mode in which the plurality of sub-pixels (P1 – P4) of a pixel are addressed simultaneously with a data signal and in a second mode in which the sub pixels (P1 – P4) of a pixel are addressed individually with respective data signals.

2. A display device according to Claim 1, wherein the device comprises drive means (40, 42, 45) for providing data signals to the column conductors and switching signals to the row conductors, and wherein the drive means is operable in the first mode to switch the switching transistors (T1 – T4) associated with the sub pixels (P1 – P4) of a pixel at the same time so as to supply a data signal on the associated column conductor (15) to each sub pixel, and wherein the drive means is operable in the second mode to switch the switching transistors associated with the sub pixels of the pixel selectively in sequence such that data signals on the associated column conductor are supplied to respective sub pixels.

3. A display device according to Claim 1 or Claim 2, wherein the sub pixels (P1 – P4) of a pixel are connected in serial manner with the input terminal of the switching transistor (T1) associated with the first sub pixel (P1) of the series being connected to the associated column address conductor (15) and with the input terminal of the switching transistor (T2 – T4) associated

with each of the other sub pixels (P2 – P4) in the series being connected to the output terminal of the switching transistor associated with the preceding sub pixel in the series.

4. A display device according to Claim 1 or Claim 2, wherein the sub pixels (P1 – P4) of a pixel are connected in parallel manner with the input terminal of the switching transistor (T1) associated with one sub pixel (P1) being connected to the associated column address conductor (15) and with the input terminals of the switching transistors (T2 – T4) associated with the other sub pixels (P2 – P4) being connected to the output terminal of the switching transistor (T1) associated with the one pixel.

5. A display device according to any one of Claims 1 to 4, wherein the control electrodes of the switching transistors (T1 – T4) associated with the sub pixels (P1 – P4) of a pixel are connected to respective different row conductors (14).

6. A display device according to any one of Claims 1 to 4, wherein each pixel (P) comprises first and second sub pixels (x + 2, x + 1; x + 4, x + 3; etc), wherein the control electrodes of the switching transistors (T4, T3) associated with the first and second sub pixels (x + 4, x + 3) of a pixel are connected to first and second row conductors (Row n + 2, Row n + 1) respectively,

wherein, for each pixel, the input of the switching transistor (T4) associated with the first sub pixel (x+4) is connected to the associated column conductor (15) and the input of the switching transistor (T3) associated with the second sub pixel (x + 3) is connected to the output of the switching transistor (T4) associated with the first sub pixel (x + 4),

wherein the first row conductor (Row n + 2) connected to one pixel (x + 3, x + 4) is connected also to the control electrode of the switching transistor (T5) associated with the second sub pixel (x + 3) of another pixel (x + 5, x + 6) connected to the associated column conductor,

and wherein the second row conductor (Row n + 1) connected to the one pixel is connected also to the control electrode of the switching transistor (T2) associated with the first sub pixel (x + 2) of a further pixel (x + 1, x + 2) connected to the associated column address conductor.

7. A display device according to any one of the preceding claims, wherein the sub pixels comprise liquid crystal picture elements connected to the outputs of their associated switching transistor.

8. A display device according to Claim 7, wherein at least two sub pixels of a pixel are of different areas.